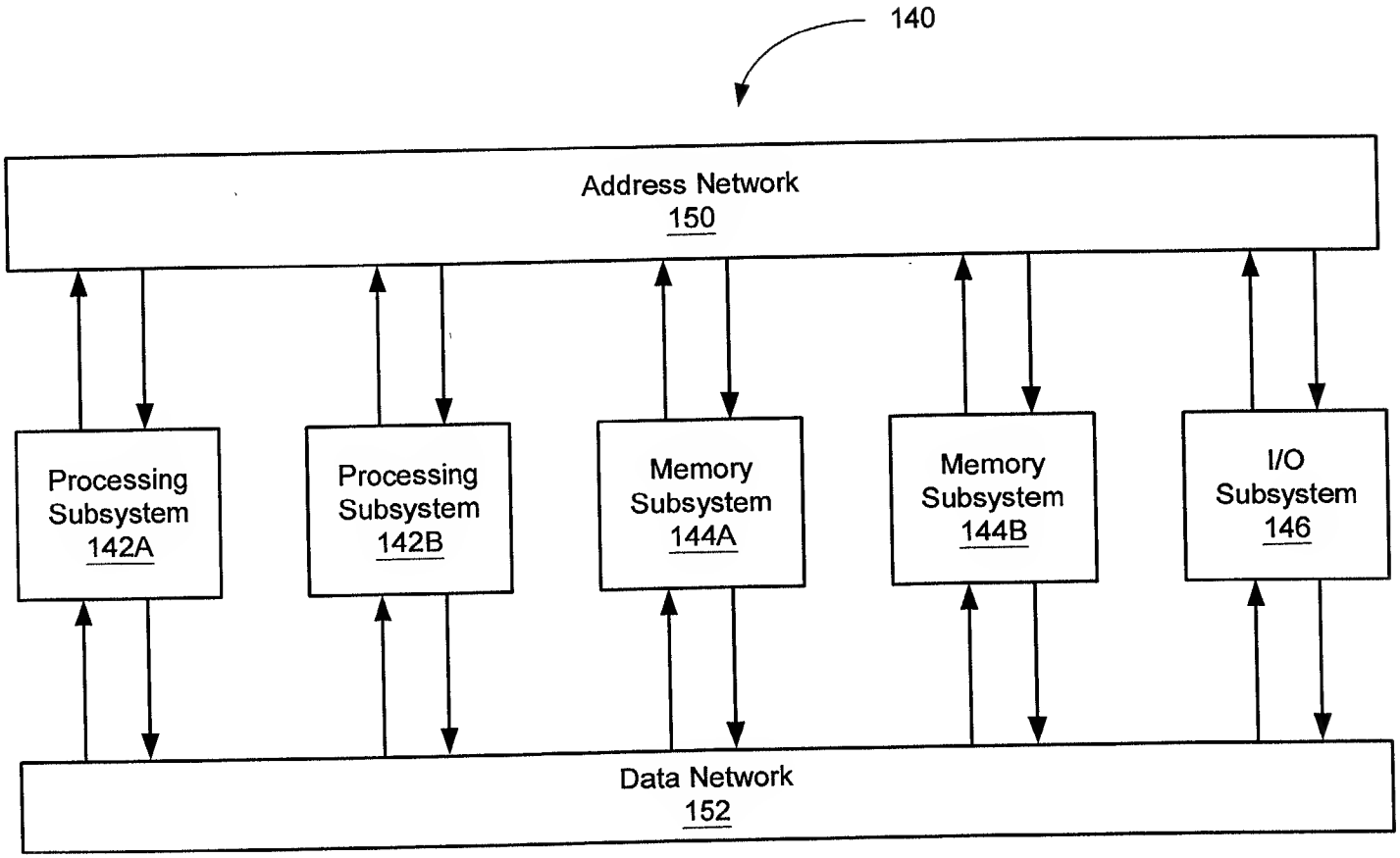


FIG. 1

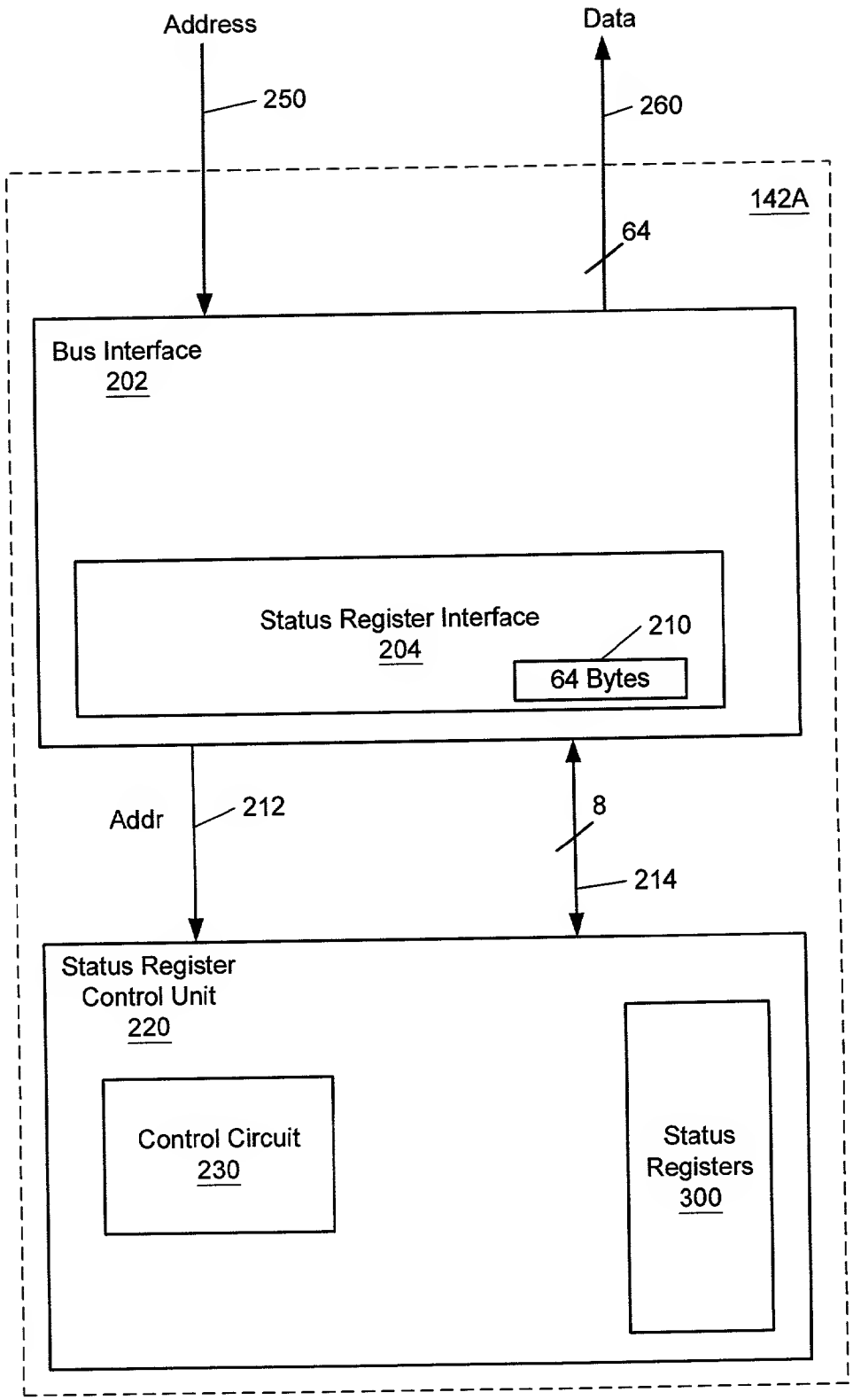

Address
250
Data
260
142A
64
Bus Interface
202
Status Register Interface
204
210
64 Bytes
Addr
212
8
214
Status Register
Control Unit
220
Control Circuit
230
Status
Registers
300

FIG. 2

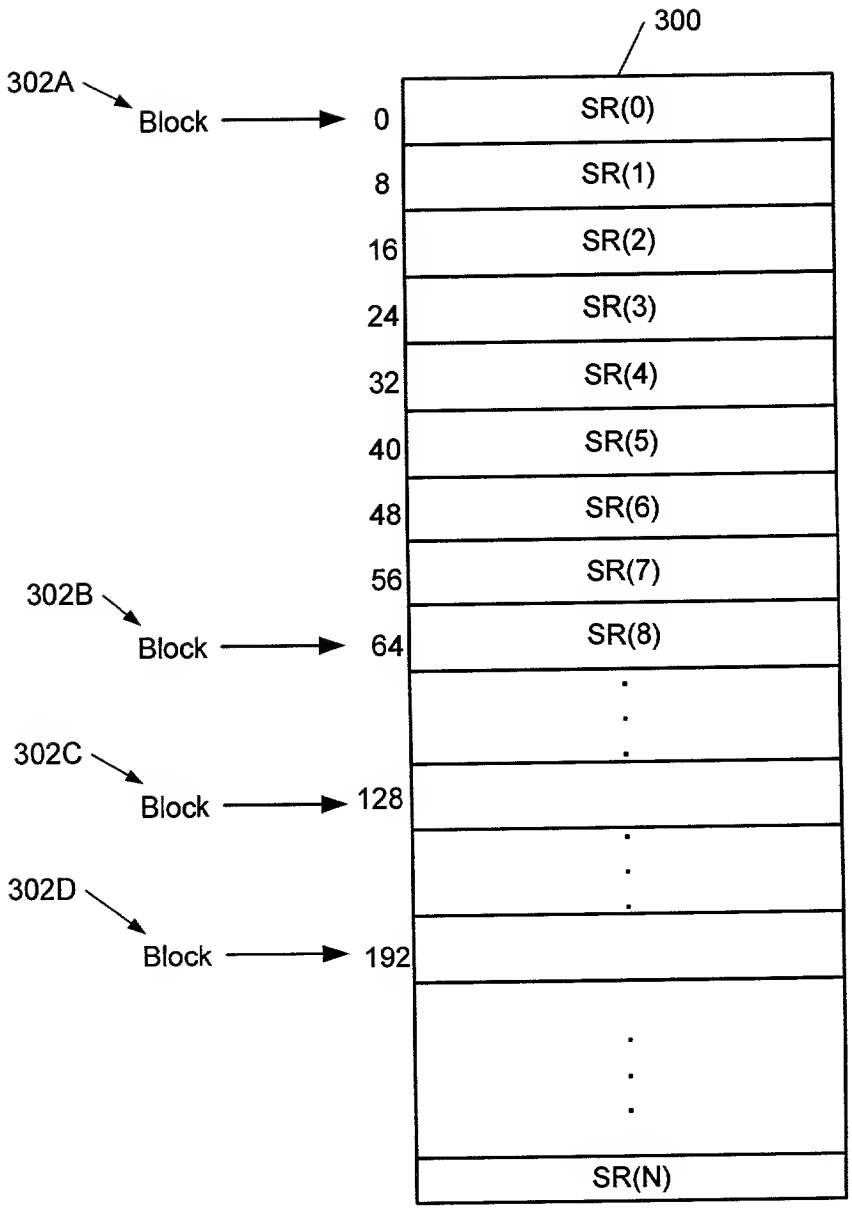
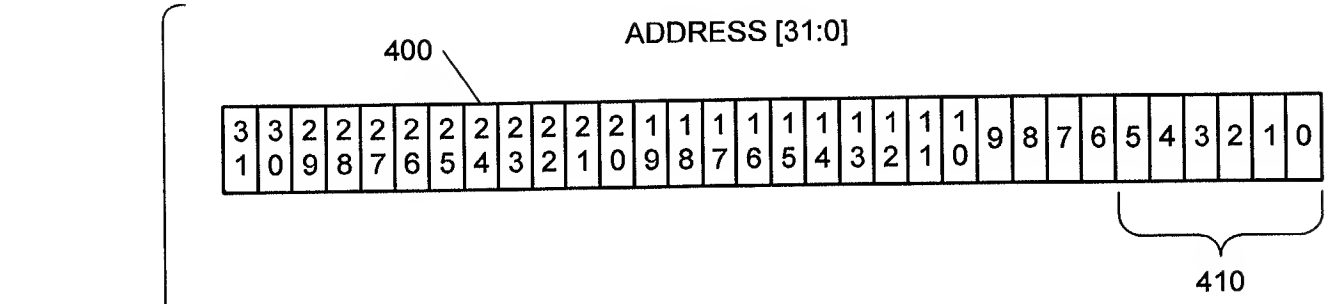

300
302A
Block
0
SR(0)
8
SR(1)
16
SR(2)
24
SR(3)
32
SR(4)
40
SR(5)
48
SR(6)
56
SR(7)
302B
Block
64
SR(8)
302C
Block
128
302D
Block
192
SR(N)

FIG. 3

FIG. 4



420

	ADDRESS [7:0]	base 10 equivalent
420A	00 000000	0
420B	01 000000	64
420C	10 000000	128
420D	11 000000	192
	. . .	. . .

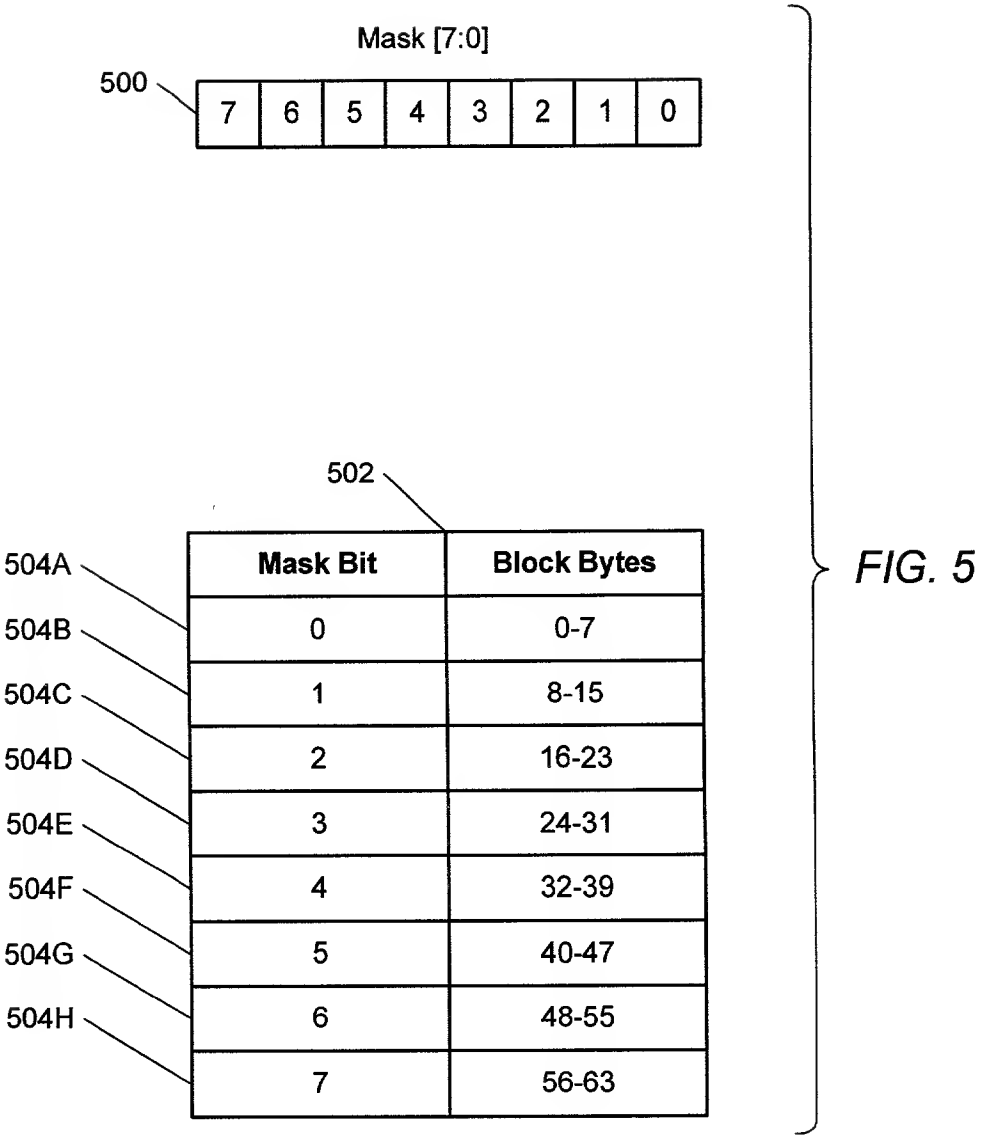

Mask [7:0]
500
7
6
5
4
3
2
1
0
502
504A
504B
504C
504D
504E
504F
504G
504H
Mask Bit
Block Bytes
0
0-7
1
8-15
2
16-23
3
24-31
4
32-39
5
40-47
6
48-55
7
56-63

FIG. 5

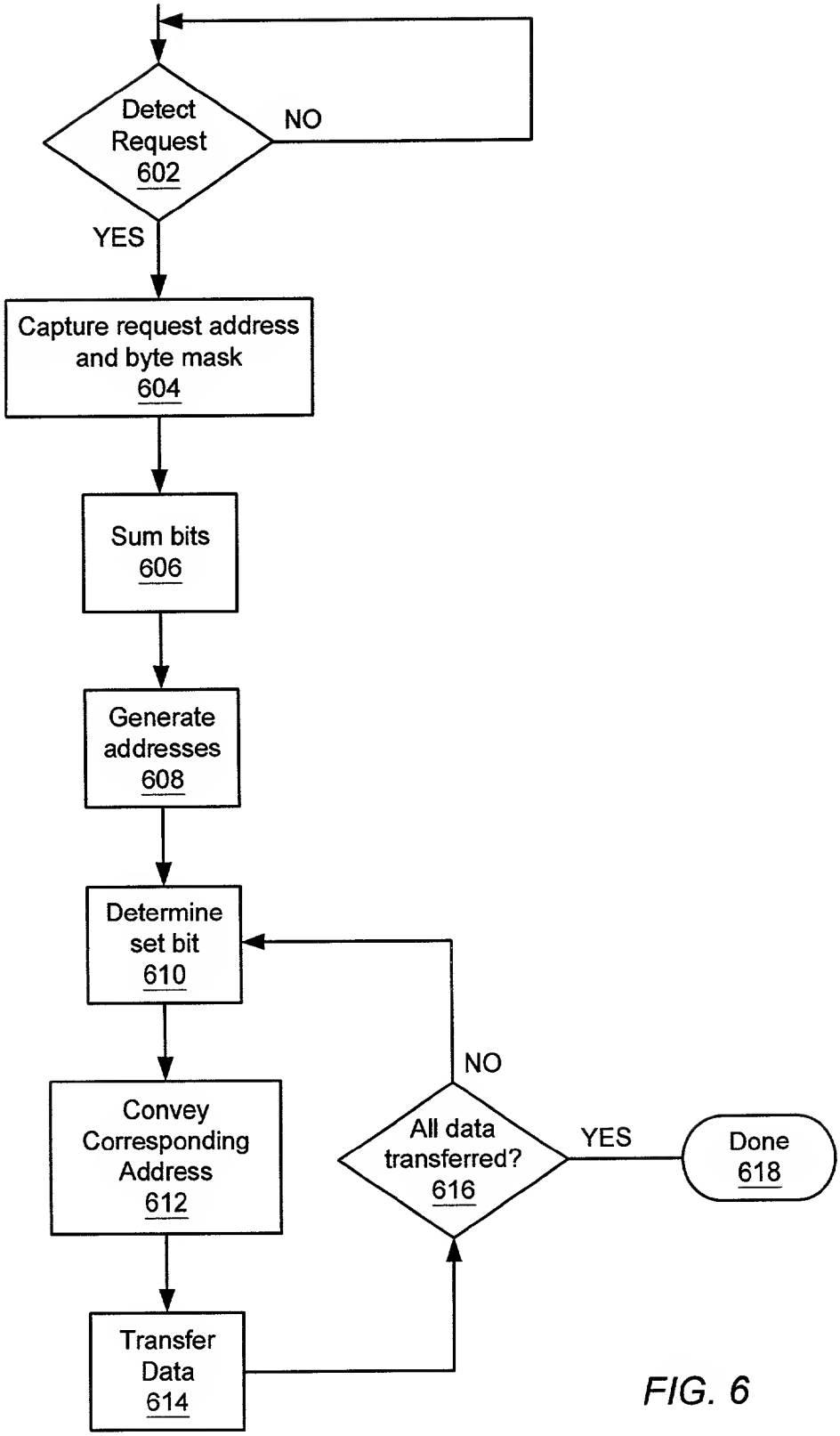

Detect Request 602
NO
YES
Capture request address and byte mask 604
Sum bits 606
Generate addresses 608
Determine set bit 610
Convey Corresponding Address 612
Transfer Data 614
All data transferred? 616
NO
YES
Done 618

FIG. 6

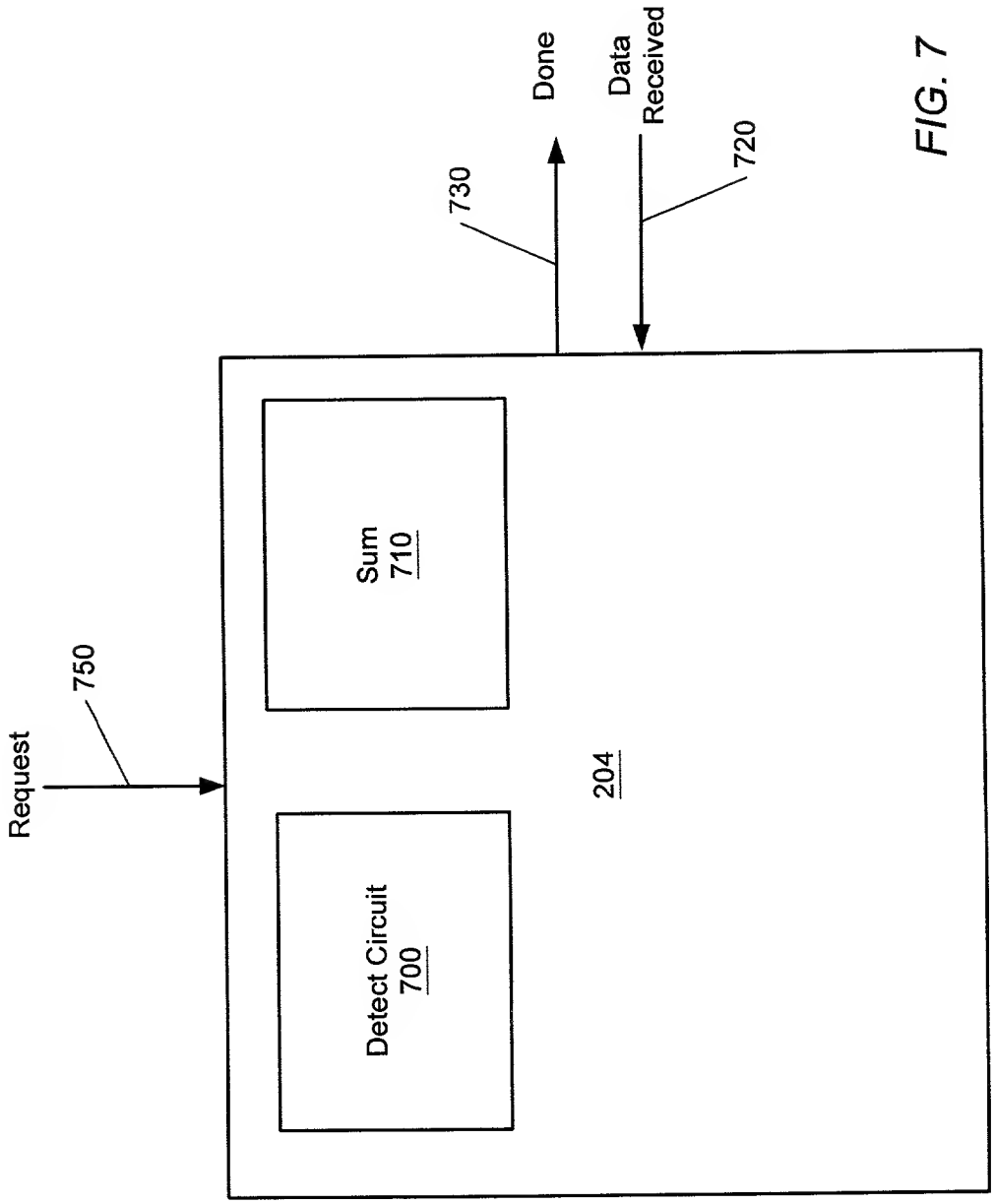

Request
750
Detect Circuit
700
Sum
710
204
730
Done
Data
Received
720

FIG. 7

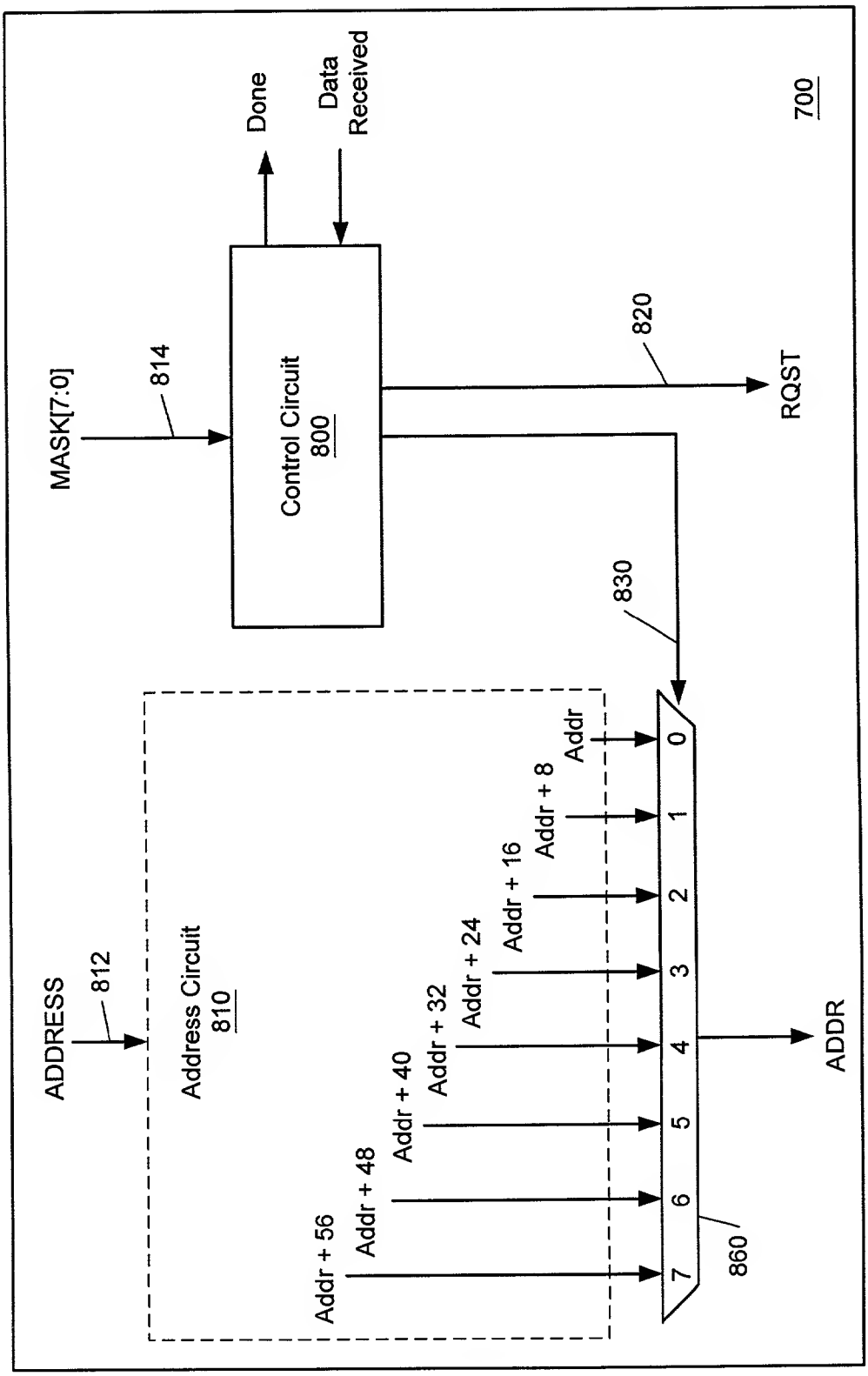

700
Done
Data Received
MASK[7:0]
814
Control Circuit
800
820
RQST
830
ADDRESS
812
Address Circuit
810
Addr
Addr + 8
Addr + 16
Addr + 24
Addr + 32
Addr + 40
Addr + 48
Addr + 56
0
1
2
3
4
5
6
7
860
ADDR

FIG. 8

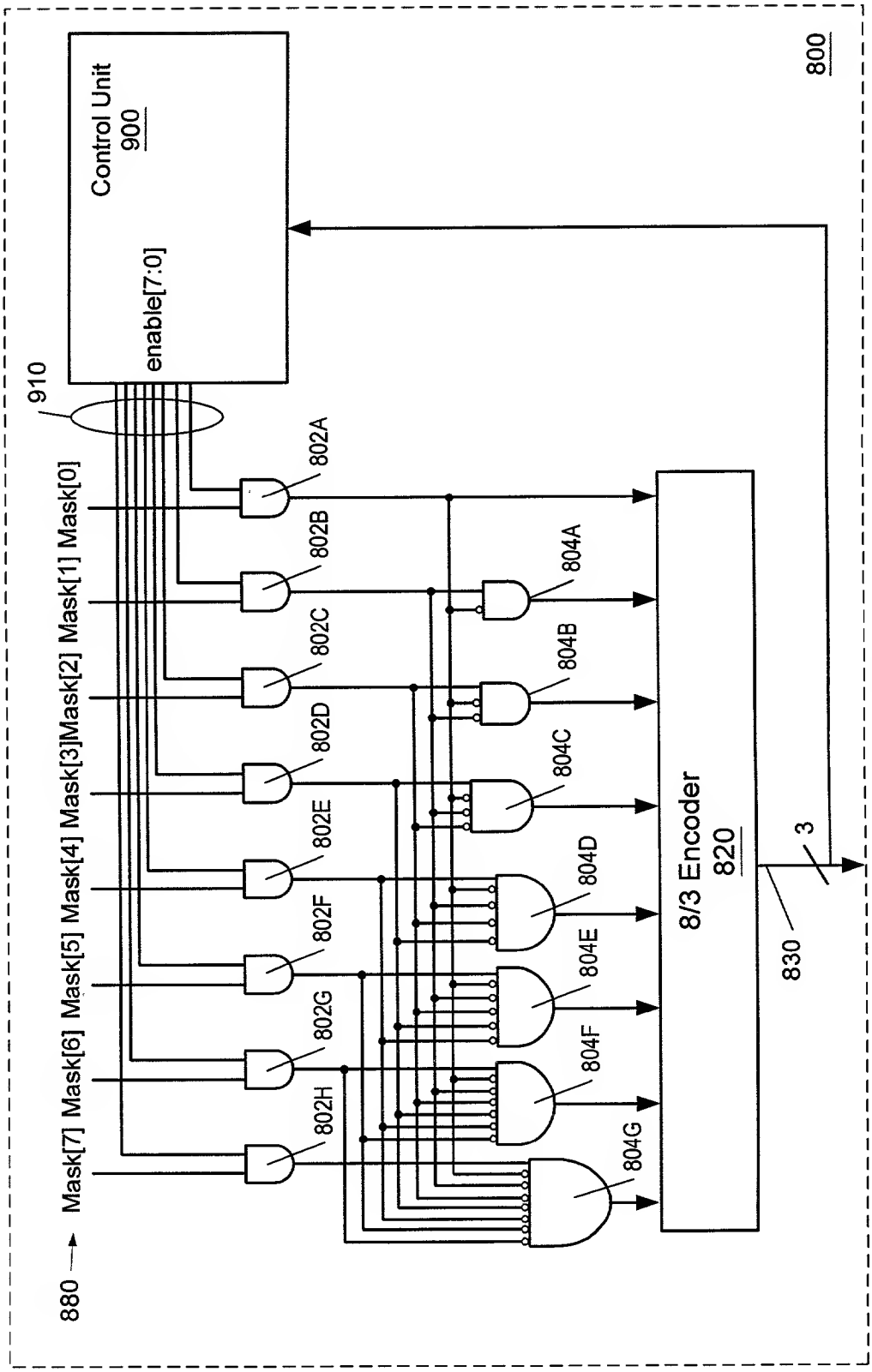
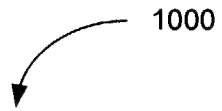

800
Control Unit
900
enable[7:0]
910
880
Mask[7] Mask[6] Mask[5] Mask[4] Mask[3]Mask[2] Mask[1] Mask[0]
802A
802B
802C
802D
802E
802F
802G
802H
804A
804B
804C
804D
804E
804F
804G
8/3 Encoder
820
3
830

FIG. 9



Iteration 1002	Enable[7:0] 1004	Mask[7:0] 1006	gates 802H-802A 1008	gates 804G-804A 1010	signal[2:0] 830 1012
0	11111111	01101000	01101000	00001000	011
1	11110000	01101000	01100000	00100000	101
2	11000000	01101000	01000000	01000000	110

FIG. 10